CLAIMS

What is claimed is

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- 2 fabricating a plurality of lands on a surface of a substrate; and
- forming an off-center via in each land.
- 1 2. The method recited in claim 1, wherein each land has a geometric center and
- 2 an edge, wherein each via has a geometric center, and wherein each via is formed
- 3 with its geometric center in a region between the geometric center and the edge of a
- 4 land.
- 1 3. The method recited in claim 2, wherein the geometric centers of vias of
- 2 adjacent lands are offset in substantially the same direction.
- 1 4. The method recited in claim 2, wherein in the forming operation the vias are
- 2 formed by drilling, and wherein the vias are drilled in a region between the
- 3 geometric center and the edge of a land.
- 1 5. The method recited in claim 4, wherein no via is drilled at the geometric
- 2 center of a land
- 1 6. The method recited in claim 4, wherein vias of adjacent lands are drilled at
- 2 substantially the same distance from the geometric centers of the respective
- lands, and wherein the offsets of such vias from the geometric centers of the
- 4 respective lands have substantially the same angle.

- 1 7. A method comprising:
- 2 fabricating a plurality of lands on a surface of a substrate;
- 3 forming an off-center via in each land;
- 4 applying a material over the surface of the substrate, including the vias, the
- 5 material comprising a thermally expansive substance;
- aligning an integrated circuit package having contacts comprising
- 7 electrically conductive material with respect to the lands; and
- 8 heating the electrically conductive material and the lands until they join.
- 1 8. The method recited in claim 7, wherein the contacts form a portion of a ball
- 2 grid array.
- 1 9. The method recited in claim 7, wherein the material comprises a volatile
- 2 organic compound.
- 1 10. The method recited in claim 7, wherein the material is from the group
- 2 comprising a solder mask, a solder flux, a solder paste, a solvent, and a via cap.
- 1 11. The method recited in claim 7, wherein the electrically conductive material
- 2 comprises solder.
- 1 12. The method recited in claim 7, wherein the contacts are solder balls.
- 1 13. The method recited in claim 7, wherein each land has a geometric center and
- 2 an edge, wherein each via has a geometric center, and wherein each via is formed
- 3 with its geometric center in a region between the geometric center and the edge of a
- 4 land.
- 1 14. The method recited in claim 13, wherein the geometric centers of vias of
- 2 adjacent lands are offset in substantially the same direction.

- 1 15. The method recited in claim 13, wherein in the forming operation the vias
- 2 are formed by drilling, wherein each land has an edge, and wherein the vias are
- 3 drilled in a region between the geometric center and the edge of a land.
- 1 16. The method recited in claim 15, wherein no via is drilled at the geometric
- 2 center of a land.
- 1 17. The method recited in claim 7, wherein in the applying operation the
- 2 thermally expansive substance is applied to the interiors of two adjacent vias, and
- 3 wherein in the heating operation the thermally expansive substance residing in the
- 4 two adjacent vias is inhibited from causing the associated contacts to be bridged
- 5 when the lands and contacts are subjected to heat.
- 1 18. A substrate comprising a plurality of lands, each land having a geometric
- 2 center, wherein each land has a via therein that is offset with respect to the
- 3 geometric center of the land.
- 1 19. The substrate recited in claim 18, wherein each land has an edge, wherein
- 2 each via has a geometric center, and wherein the geometric center of each via is in a
- 3 region between the geometric center and the edge of its associated land.
- 1 20. The substrate recited in claim 19, wherein the geometric centers of vias of
- 2 adjacent lands are offset in substantially the same direction.
- 1 21. An electronic assembly comprising:
- 2 an integrated circuit package; and
- a substrate having a plurality of lands, each land having an offset via, and
- 4 each land being aligned with respect to a contact of the integrated circuit package.

- 1 22. The electronic assembly recited in claim 21, wherein each via inhibits a
- 2 thermally expansive substance residing in the vias from causing adjacent contacts of
- 3 the integrated circuit package to be bridged when the lands and contacts are
- 4 subjected to heat.
- 1 23. The electronic assembly recited in claim 22, wherein the thermally
- 2 expansive substance comprises a volatile organic compound.
- 1 24. The electronic assembly recited in claim 22, wherein the thermally
- 2 expansive substance comprises a volatile liquid that forms a portion of a material
- 3 from the group consisting of a solder mask, a solder flux, a solder paste, a solvent,
- 4 and a via cap.
- 1 25. The electronic assembly recited in claim 21, wherein the lands comprise a
- 2 first group having vias offset in a first direction, and a second group having vias
- 3 offset in a second direction.
- 1 26. The electronic assembly recited in claim 21, wherein each land has a
- 2 geometric center and an edge, wherein each via has a geometric center, and wherein
- 3 each via is formed with its geometric center in a region between the geometric
- 4 center and the edge of a land.
- 1 27. The electronic assembly recited in claim 26, wherein the geometric centers
- 2 of vias of adjacent lands are offset from the geometric centers of such lands in the
- 3 same direction.
- 1 28. An electronic system comprising an electronic assembly having an
- 2 integrated circuit package, and a substrate having a plurality of lands, each land
- 3 being aligned with respect to a respective contact of the integrated circuit package
- 4 and comprising an offset via.

- 1 29. The electronic system recited in claim 28, wherein each land has a geometric
- 2 center and an edge, wherein each via has a geometric center, and wherein the
- 3 geometric center of each via is in a region between the geometric center and the
- 4 edge of a land.
- 1 30. The electronic system recited in claim 29, wherein the geometric centers of
- 2 vias of adjacent lands are offset from the geometric centers of such lands in the
- 3 same direction.

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